In the Specification

Please substitute the following amended paragraphs for the paragraphs beginning on page 5, lines 17.

As shown in FIG. 2A, a dielectric layer is blanketly formed as a buffer layer 210, such as a silicon oxide layer, covering a surface of a TFT array glass substrate 200. A gate oxide layer 220 is blanketly deposited on the surface of the buffer layer 210. A patterned metal layer 230, having a first and second end, is formed on the surface of the gate oxide layer 220, wherein the direction extending from the first end to the second end is parallel to the substrate 200 surface. The patterned metal layer 230 may be formed simultaneously with gate metal process.

Another dielectric layer 240 with a flat surface is then formed, covering the surface of the metal layer 230 and the gate oxide layer 220, as an interlayer dielectric (ILD) layer. At least two via holes 241 and 242 parallel to extending direction of the metal layer 230 are formed inline in the dielectric layer 240, exposing the underlying metal layer 230 as shown in FIG. 2B.

Please substitute the following amended paragraph for the paragraph beginning on page 7, lines 27.

FIG. 3B is a cross-section of FIG. 3A along line 1-1. A dielectric layer 310, such as a laminated oxide layer, is formed on a substrate, e.g. a TFT array substrate 300 for an LCD panel. Metal layer 330 is formed and pattered on the dielectric layer 310 as a conductive line, wherein the direction extending from one end of the metal layer 330 to the other end thereof is parallel to the substrate surface. Another flat dielectric layer 340 is formed on the dielectric layer 310 and covers

the metal layer 330. Two via holes parallel to extending direction of the metal layer 330 are formed in the dielectric layer 340 above and exposing one end of the metal layer 310.